IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) Test equipment for an LSI as a device under test, which compares an output signal output from the LSI to be measured as data to be measured with predetermined expectation value data to judge whether or not the LSI to be measured is failure, the ~~device~~ test equipment comprising:

a first LSI tester which inputs a first signal output from the LSI to be measured and which acquires the first signal by a plurality of strobes having a certain timing interval to output level data in a time series, the first LSI tester having a first time interpolator which is comprised of:

a sequential circuit which inputs the first signal output from the LSI to be measured;

a delay circuit which successively inputs a strobe delayed at a certain timing interval into the sequential circuit to output the level data of the time series from the sequential circuit; and

an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the clock of the LSI to be measured to output the data;

a second LSI tester which inputs a second signal output from the LSI to be measured and which acquires the second

signal by a plurality of strobes having a certain timing interval to output level data in a time series, the second LSI tester having a second time interpolator which is comprised of:

a sequential circuit which inputs the second signal output from the LSI to be measured; and

a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series; and

a selection circuit which is disposed in at least one of the first and second LSI testers and which inputs the level data of the time series output from the first and second LSI testers to select the second signal input into the second LSI tester at a timing of the first signal input into the first LSI tester and which outputs the second signal as the data to be measured of the LSI to be measured, the selection circuit comprising a selector which selects one data from the level data of the time series input from the second time interpolator using the level data of the time series coded by the first time interpolator as a selection signal to output data to be measured of the LSI to be measured.

2. (currently amended) The test equipment for the LSI as a device under test according to claim 1, wherein ~~the first LSI tester comprises a first time interpolator including:~~

~~a sequential circuit which inputs a clock output from the LSI to be measured;~~

~~a delay circuit which successively inputs a strobe delayed at a certain timing interval into the sequential circuit to output the level data of the time series from the sequential circuit; and~~

~~an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the clock of the LSI to be measured to output the data,~~

~~the second LSI tester comprises a second time interpolator including:~~

~~a sequential circuit which inputs the output data output from the LSI to be measured; and~~

~~a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series, and~~

~~the selection circuit comprises a selector which selects one data from the level data of the time series input from the second time interpolator using the level data of the time series coded by the first time interpolator as a selection signal to output data to be measured of the LSI to be measured~~ the first signal is a clock from the LSI to be measured, and the second signal is output data from the LSI to be measured.

3. (currently amended) The test equipment for the LSI as a device under test according to ~~claim 2~~ claim 1, wherein the second time interpolator includes an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating the edge timing of the output data of the LSI to be measured to output the timing data.

4. (currently amended) The test equipment for the LSI as a device under test according to claim 1, further comprising a bus which is connected to the first and second LSI testers and which distributes data output from the first and second LSI testers to a predetermined selection circuit.

5. (currently amended) A jitter analyzer for an LSI as a device under test, which acquires/analyzes ~~a~~ distribution of jitters of an output signal ~~output~~ from the LSI to be measured, comprising:

a first LSI tester which inputs the output signal output from the LSI to be measured and which acquires the output signal by a plurality of strobes having certain timing intervals to output level data in a time series; and

jitter distribution analysis means for inputting the level data of the time series output from the first LSI tester to acquire a timing of the output signal input into the first LSI tester and for outputting the distribution of the jitters of the output signal;

wherein the first LSI tester has a first time interpolator which is comprised of:

a sequential circuit which inputs the first signal output from the LSI to be measured;

a delay circuit which successively inputs a strobe delayed at a certain timing interval into the sequential circuit to output the level data of the time series from the sequential circuit; and

an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the clock of the LSI to be measured to output the data.

6. (canceled)

7. (previously amended) The jitter analyzer for the LSI as a device under test according to claim 5, wherein the jitter distribution analysis means comprises a storage circuit which stores the timing data output from the encoder, and

the jitter analyzer acquires the distribution of edge timings of output signals input into the first LSI tester from a plurality of data stored in the storage circuit.

8. (previously amended) The jitter analyzer for the LSI as a device under test according to claim 5, wherein the jitter distribution analysis means comprises:

a decoder which inputs the timing data output from the encoder and which decodes the timing data into the level data of the time series to output the level data; and

a plurality of counters which count the output signals of the decoder for each output terminal, and

the jitter analyzer acquires a distribution of edge timings of the output signals input into the first LSI tester from a plurality of data output from the counter.

9. (original) A phase difference detector for an LSI as a device under test, which detects a phase difference between first and second signals output from the LSI to be measured, comprising:

a first LSI tester which inputs a first signal output from the LSI to be measured and which acquires the first signal as data by a plurality of strobes having a certain timing interval to output level data in a time series, the first LSI tester having a first time interpolator which is comprised of:

a sequential circuit which inputs the first signal output from the LSI to be measured;

a delay circuit which successively inputs a strobe delayed at a certain timing interval into the sequential circuit to output the level data of the time series from the sequential circuit; and

an encoder which inputs the level data of the time series output from the sequential circuit and which

encodes the level data into timing data indicating an edge timing of the clock of the LSI to be measured to output the data;

a second LSI tester which inputs a second signal output from the LSI to be measured and which acquires the second signal as data by a plurality of strobes having a certain timing interval to output level data in a time series, the second LSI tester having a second time interpolator which is comprised of:

a sequential circuit which inputs the second signal output from the LSI to be measured; and

a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series; and

a phase difference detection circuit which is disposed in at least one of the first and second LSI testers and which inputs the level data of the time series output from the first and second LSI testers to calculate a difference between a timing of the first signal input into the first LSI tester and that of the second signal input into the second LSI tester and which outputs the phase difference.

10. (original) The phase difference detector for the LSI as a device under test according to claim 9, wherein ~~the first LSI tester comprises a first time interpolator including:~~

~~a sequential circuit which inputs a clock output from the LSI to be measured;~~

~~a delay circuit which successively inputs a strobe delayed at a certain timing interval into the sequential circuit to output the level data of the time series from the sequential circuit; and~~

~~an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the clock of the LSI to be measured to output the timing data,~~

~~the second LSI tester comprises a second time interpolator including:~~

~~a sequential circuit which inputs the output data output from the LSI to be measured;~~

~~a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series; and~~

~~an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the output data of the LSI to be measured to output the timing data, and~~

the phase difference detection circuit comprises:

a calculation circuit which subtracts the level data of the time series encoded by the first time interpolator and the

level data of the time series encoded by the second time interpolator; and

a decoder which decodes a calculation result of the calculation circuit, and

the phase difference detector outputs the data decoded by the decoder as a phase difference between the clock and output data of the LSI to be measured.

11. (currently amended) The phase difference detector for the LSI as a device under test according to claim 10, wherein the phase difference detection circuit comprises a plurality of counters which count output signals of the decoder for each output terminal, and

the phase difference detector acquires ~~a~~ distribution of phase differences between the clock input into the first LSI tester and the output data input from the second LSI tester from a plurality of data output from the counter.

12. (currently amended) The phase difference detector for the LSI as a device under test according to claim 9, ~~comprising:~~ further comprising a bus which is connected to the first and second LSI testers and which distributes data output from the first and second LSI testers to a predetermined phase difference detection circuit.